V. Remarks

A. Claim Objections

The Action objects to Claims 6-7 and 19-22 because they were not presented in a single paragraph. Applicants have corrected this informality, which was due to a formatting error, by presenting a new listing of the claims where claims 6, 7, 19, 20 and 21 are each presented as individual paragraphs. Reconsideration and withdrawal of the objection to the claims are respectfully requested.

B. Summary of Amendments to the Specification

Paragraph 1 has been amended to include the serial number of the first referenced patent application, as well as its filing date. References to attorney docket numbers have been deleted. The patent number of the second referenced patent application and full title have also be provided. It is submitted that this amendment addresses the Examiner's objection to the Specification set forth in the Office Action.

Paragraph 6 has been amended to correct a typographical error in the recitation of "e.g.", specifically to remove an extra period (".").

The first paragraph of the "Brief Description of the Drawings" section was amended to recite paragraph "0011a" rather than paragraph "0001" and to correct the description of FIGS. 2a, 2b and FIGS. 3a, 3B, as FIGS. 2a and 3a show PMOS access transistors and FIGS. 2b and 3b shown NMOS access transistors.

Paragraph 23 has been amended to correct "p-channel" to "n-channel" and "PMOS" to "NMOS" consistent with the circuit diagram of FIG. 3.

Paragraph 25 has been amended to better reflect that FIG. 4 shows both PMOS and NMOS access transistors.

C. Rejection under 35 U.S.C. §112

The Action rejects Claims 1-22 as failing to comply with the enablement requirement. The Examiner states that it is not understood how the source of N-channel transistor M1 in FIGS. 2a and 2b "is interconnected or it is floated/opened." Similar comments are provided respective to the transistor M1 of the circuit of FIGS. 3a and 3b and transistors M1 and M2 of the circuit of FIG. 4. Reconsideration and withdrawal of the rejection of these claims are respectfully requested in view of the following arguments.

"The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." MPEP 2164.01 (citing United States v. Telectronics, Inc., 857 F.2d 778, 785 (Fed. Cir. 1988)). It is submitted that the description is sufficient on its own, or in connection with the knowledge in the art, to allow one of ordinary skill to make and use the invention.

With respect to the illustrated embodiments of FIGS. 2a, 2b, 3a, 3b and 4, one of ordinary skill would understand that the terminals identified by the examiner are neither opened nor floated. As explained in the specification, the current mirrors including the transistors identified by the Examiner are configured to extract leakage current (or multiple thereof) from monitored cells and create a current flow that can be monitored and used. (See, e.g., Paragraph 21). In one example, the current can be used to dynamically and in real-time determine the refresh period dependent upon a variety of operating environment conditions discerned from the leakage current. (See, e.g., Paragraph 26) Or, in one embodiment, the output can simply be used as a current source. (See id.).

The illustrated embodiments act like a current source, so they would sink a current for (e.g., FIG. 2a, 2b, FIG. 4) or supply a current to (e.g., FIG. 3a, 3b) the selected circuit connected to the terminal. To what circuit the noted terminal of transistor M1 (FIGS. 2, 3) or transistor M2 (FIG. 4) is connected depends on how the current is to be used. The terminal could, for example,

be connected to any current control circuitry, such as a current control oscillator, current control level detection circuit, temperature sensor, etc. depending on its use.

Using Claim 1 as an example, Claim 1 recites as an element a current mirror "operable to mirror a total leakage current from said plurality of bit cell access transistors when said access transistors are biased to simulate said inactive bit cells." Per the discussion above, one of ordinary skill is certainly provided examples of how to make such a current mirror in FIGS. 2 and 3 and the accompanying description. Examples are given in the description as to how to use the generated current and operable circuits are known to those in art. It is respectfully submitted that one of ordinary skill would appreciate this point and that the description is sufficient to enable one of ordinary skill in the art to both make and use the claimed inventions in compliance with §112, ¶1.

Per the foregoing, reconsideration and withdrawal of the rejection of the claims are respectfully requested.

VI. Conclusion

In view of the foregoing remarks and amendments, Applicant(s) submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

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IV. Amendments to the Drawings

Formal drawings are submitted with this response and are captioned "Replacement Sheets."